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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/082,581 | 05/21/1998 | KENJI NAGASE | 980673 | 2888 |

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| WHIPKEY, JASON T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2612 | |

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/082,581 | NAGASE, KENJI | |
| | Examiner | Art Unit | |
| | Jason T. Whipkey | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,7 and 8* is/are allowed.

6)☒ Claim(s) *1-3 and 6* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed October 7, 2004, have been fully considered but they are not persuasive.

Regarding Applicant's arguments against the rejection of claim 1 (and presumably, claim 6), Applicant notes in the last paragraph on page 3 that part 3 in Ibori is not a semiconductor switching element. As Applicant correctly noted, the examiner intended to cite part 11 as the semiconductor switching element. The examiner apologizes for the error.

Applicant argues in the next-to-last paragraph on page 4 that "Ibori is not concerned at all with short circuiting positive line P and negative line N upon application of signal 'a' or 'b' to on-off control circuit 12" (emphasis in original).

Applicant correctly notes in the following paragraph that "the semiconductor switch 11 of Ibori short-circuits the line P and the line N which are included in a single circuit." Applicant also correctly notes that "the discharge of smoothing capacitor 3 ... can be delayed within the allowable duration time (signal 'b') when a.c. power is interrupted". However, Applicant's arguments fail to make the connection that the short-circuiting of lines P and N occurs *in response to* the interruption of AC power, which is what is claimed. While the short-circuiting is not instantaneous, it does occur after a prescribed delay *in response to* the interruption of AC power (see column 4, lines 14-18).

Regarding Applicant's arguments on page 5, while Ibori is silent with regard to separate first and second circuits generating the positive and negative polarity voltages, respectively, this limitation is taught by Josephson.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Josephson (U.S. Patent No. 4,608,625) in view of Ibori (U.S. Patent No. 5,465,202).

Regarding claim 1, Josephson discloses a power supply circuit, shown in Figure 1, with a first circuit for producing a positive polarity voltage at +12 V and +5 V output terminals, shown on the right side of the figure. This first circuit consists of rectifier 48, which includes capacitors 62 and 66 (column 4, lines 41-50), and a chopper circuit, which consists of electrical switch means 44 and transistor switch 24. Switch 24 turns on and off repeatedly to create a "chopped" output from transformer 22 (column 3, lines 44-52, and column 4, lines 13-27).

A second circuit, consisting of rectifier 16, diode 110, and capacitors 114 and 118, produces a negative polarity voltage of -12 V at an output terminal, shown on the right side of

Figure 1. Ground terminal GND, also shown on the right side of Figure 1, provides a reference for the positive and negative terminals.

Josephson is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power.

Ibori discloses an electric discharge apparatus. As shown in Figure 3, semiconductor switching element 3 short-circuits positive line P and negative line N upon application of a signal from on-off control circuit 12 ("a power-off signal supplied by [a] control circuit"). On-off control circuit 12 receives signal b from input power detecting circuit 13, which detects the off state of the system's power source.

As stated in column 1, lines 18-19, an advantage to short-circuiting the positive and negative lines upon loss of power is that electrical shock by residual voltage may be prevented. For this reason, it would have been obvious at the time of invention to have Josephson's system short-circuit the positive and negative terminals upon loss of the power supply.

Regarding claims 2 and 3, transistor 11 in Ibori is a switching element, and resistor 10 is a current-limiting element. Both are located between the positive and negative terminals.

4. Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sawanobori in view of Ibori and further in view of Takeda (U.S. Patent No. 5,475,500).

Sawanobori shows that CCD 15 uses a power supply 15 consisting of a 15V line and a -9V line (Drawing 1). When power is lost on -9V line S3, discharge circuit 18 discharges the line to prevent "deterioration or destruction of the image pickup element due to application of a negative voltage" (constitution, lines 15-21). Therefore, the significant teachings provided by

Sawanobori are: (a) that CCDs may require power supplies outputting separate positive and negative voltages, and (b) that a discharge circuit may prevent deterioration of or destruction to a CCD.

Sawanobori is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power.

Ibori discloses an electric discharge apparatus. As shown in Figure 3, semiconductor switching element 3 short-circuits positive line P and negative line N upon application of a signal from on-off control circuit 12. On-off control circuit 12 receives signal b from input power detecting circuit 13, which detects the off state of the system's power source.

As stated in column 1, lines 18-19, an advantage to short-circuiting the positive and negative lines upon loss of power is that electrical shock by residual voltage may be prevented. For this reason, it would have been obvious at the time of invention to have Sawanobori's system short-circuit the positive and negative terminals upon loss of the power supply.

Ibori is silent with regard to including a microcomputer and using it to produce the power-off signal.

Takeda discloses an imaging device controlled by microcomputer 16. As shown in the flowchart of Figure 7B, when microcomputer 16 detects a power off command (column 7, lines 58-65), it initiates a shutdown procedure for power supply parts 2a, 4, and 5 (column 8, lines 28-41). An advantage to using a microcomputer to produce a power-off signal is that the circuitry used to control the signal may be reused during other operations, thus simplifying the hardware design. For this reason, it would have been obvious at the time of invention to have Ibori perform shutdown control using a microcomputer.

***Allowable Subject Matter***

5. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests the power supply circuit described, particularly one with a first output terminal connected to a chopper circuit and a second output terminal connected to a fly-back circuit, wherein the second terminal has no connection to the chopper circuit.

6. Claims 5, 7, and 8 are allowed.

Regarding each of these claims, no prior art could be located that teaches or fairly suggests the power supply circuit described, particularly one with a first output terminal connected to a chopper circuit and a second output terminal connected to a fly-back circuit, wherein the second terminal has no connection to the chopper circuit.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern standard time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber, can be reached at (571) 272-7308. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW

JTW
March 9, 2005

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600